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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)																
<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]</p> <p>on <u>March 14, 2006</u></p> <p>Signature <u></u></p> <p>Typed or printed name <u>Edouard Garcia</u></p>		Application Number	Filed															
		10/820,484	April 8, 2004															
		First Named Inventor																
		Michael G. Kelly																
Art Unit		Examiner																
2826		Andujar, Leonardo																
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <table border="0"><tr><td><input type="checkbox"/> applicant/inventor.</td><td><u></u></td></tr><tr><td><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</td><td>Signature Edouard Garcia</td></tr><tr><td><input checked="" type="checkbox"/> attorney or agent of record. 38,461</td><td>Typed or printed name</td></tr><tr><td>Registration number _____</td><td>(650) 289-0904</td></tr><tr><td></td><td>Telephone number</td></tr><tr><td><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34.</td><td>March 14, 2006</td></tr><tr><td>Registration number if acting under 37 CFR 1.34 _____</td><td>Date</td></tr></table> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p> <table border="1"><tr><td><input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.</td></tr></table>				<input type="checkbox"/> applicant/inventor.	<u></u>	<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	Signature Edouard Garcia	<input checked="" type="checkbox"/> attorney or agent of record. 38,461	Typed or printed name	Registration number _____	(650) 289-0904		Telephone number	<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34.	March 14, 2006	Registration number if acting under 37 CFR 1.34 _____	Date	<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Michael G. Kelly
Serial No. : 10/820,484
Filed : April 8, 2004
Title : THERMAL DISSIPATION IN INTEGRATED CIRCUIT SYSTEMS

Art Unit : 2826
Examiner : Andujar, Leonardo

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1-21 are pending and the subject of this Pre-Appeal Brief Request for Review.

I. Claims 1-9, 15-17, and 21

Claims 1-9, 15-17, and 21 are rejected under 35 U.S.C. § 103(a) over White (U.S. 5,665,655) in view of Dias (U.S. 6,812,548).

A. Independent claim 1

In support of his rejection of claim 1, the Examiner stated that FIG. 25 of White shows "an integrated circuit system, comprising: a die 1 incorporating an integrated circuit 2 and having a top side and a bottom side, the top side supporting an electrical signal metallization 6 and a top side thermal dissipation metallization 9"

Element 9, however, is not a thermal dissipation metallization that is supported by a top side of a die, it is instead a buried electrical interconnect that is connected to the active region 2 by a tungsten contact 6 (see, e.g., FIG. 25, col. 5, line 63, and col. 10, line, 12). As shown in FIG. 25, element 9 forms part of the electrical signal metallization that includes interconnects 9, 39, 46 and contacts 6, 38, 44. One skilled in the art at the time the invention was made would not have considered the electrical interconnect 9 to be a "thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term, because the electrical interconnect 9 is buried under dielectric layers that would interfere with heat dissipation and because the reasonably expected dimensions of the buried electrical interconnect 9 would not be sufficient to produce any appreciable thermal dissipation in the dice disclosed in White. The Examiner has not identified any element in White's disclosure

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Edouard Garcia

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that one skilled in the art reasonably would have considered to be "a thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term.

In apparent response to the point that interconnect 9 is a buried layer, the Examiner stated that "White's figure 25 clearly shows that the element 9 is atop the thermal dissipation metallization 6." This statement, however, is inconsistent with the Examiner's assertion that element 6 corresponds to the electrical signal metallization recited in claim 1. Moreover, this statement does not address the point that interconnect 9 is not a "thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term.

Dias does not make-up for the failure of White to teach or suggest a thermal dissipation metallization that is supported by a top side of a die of an integrated circuit system, as recited in claim 1. Dias discloses that the top side of the die corresponds to the topmost one of the alternating layers 112 of dielectric material and patterned electrically conducting material (see col. 4, lines 4-12). Dias does not specify whether the top interconnect layer is a dielectric material or a patterned electrically conductive material. In accordance with the knowledge generally available, however, one skilled in the art would have understood that the topmost layer of an interconnect layer stack of the type disclosed in Dias would have been a dielectric passivation layer (see, e.g., the passivation layer 48 shown in FIG. 25 of White). In addition, one skilled in the art at the time the invention was made would not have expected the patterned electrical interconnects disclosed in Dias to have dimensions that are sufficient to produce any appreciable thermal dissipation in the integrated circuit system dice disclosed in Dias. For these reasons, one skilled in the art at the time the invention was made would not have had any reasonable basis to believe that Dias' die includes a thermal dissipation metallization that is supported by a top side of a die of an integrated circuit system, as recited in claim 1.

Thus, neither White nor Dias teaches or suggests an integrated circuit system that includes a thermal dissipation metallization supported by a top side of a die and a thermal dissipation metallization supported by a bottom side of the die. Therefore, the combination of White and Dias cannot possibly teach or suggest the invention defined by independent claim 1. For at least these reasons, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

The Examiner also has stated that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a bottom side thermal dissipation

metallization layer in the back surface of the die disclosed in White to facilitate the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interface materials do not wet (i.e., stick to) semiconductor wafers as taught by Dias.” The Examiner, however, has not explained why one skilled in the art would have been motivated to attach a heat spreader to the back side of White’s die in the first place. Indeed, assuming for the purpose of argument only that the Examiner’s factually incorrect assertion that the buried interconnect 9 in White’s die is a top side thermal dissipation metallization, what would have motivated one skilled in the art at the time the invention was made to attach a second thermal dissipation metallization to the back side of White’s die? The Examiner’s response in ¶ 35 of the final Office action does not address this point. Moreover, White does not teach or suggest anything about the desirability of attaching heat spreaders to the top or bottom sides of a die, Dias only teaches attaching a single heat spreader to the back side of an integrated circuit die, and the Examiner’s reliance on well-known knowledge in ¶ 35 of the final Office action amounts to no more than the impermissible “obvious to try” rationale for finding obviousness.

For these reasons, it appears that the Examiner improperly has engaged in hindsight reconstruction of the claimed invention, using applicants’ disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper *prima facie* case of obviousness and the rejection of claim 1 should be withdrawn for this additional reason.

B. Dependent claims 2-9 and 21

Each of claims 2-9 and 21 incorporates the features of independent claim 1 and therefore is patentable over White and Dias for at least the same reasons explained above. In addition, the Examiner’s statement regarding claim 8 in ¶ 11 of the final action is incorrect since the contact 38 clearly is not a through-hole of the interconnect 9, and the Examiner’s statement regarding claim 21 in ¶ 13 of the final action is incorrect since the contact 6 is connected directly to the interconnect 9.

C. Independent claim 15

Claim 15 is patentable over White and Dias for at least the same reasons explained above in connection with independent claim 1. In addition, the Examiner has stated that the

contact 6 corresponds to the "exposed electrical signal communication metallization" and the interconnect 9 corresponds to the "exposed top side thermal dissipation metallization."

Contrary to the Examiner's statement, however, FIG. 25 clearly shows that contact 6 and interconnect 9 both are buried under a number of overlying layers. Thus, neither contact 6 nor interconnect 9 is "exposed" in accordance with any reasonable interpretation of the term.

II. Claims 10 and 11

Claims 10 and 11 are rejected under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo (U.S. 6,717,267). The Examiner has stated that Kunikiyo "shows a top heat spreader 32 metallurgically bonded (31) to the top side thermal dissipation metallization of the die (dummy pattern 25a)." Kunikiyo discloses attaching a single heat sink 32 to an integrated circuit die. Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31, as recited in claim 10. The Examiner did not address this point in the final Office action. For at least these reasons the Examiner's rejection of claims 10 and 11 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo should be withdrawn.

III. Claims 12 and 13

Claims 12 and 13 are rejected under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang (U.S. 5,977,626). Each of claims 12 and 13 incorporates the features of claim 10. Wang does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. To the contrary, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53). For at least these reasons the Examiner's rejection of claims 12 and 13 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang should be withdrawn.

IV. Claim 14

Claim 14 is rejected under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Khan (U.S. 6,853,070). Claim 14 incorporates the features of independent claim 10. Khan does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. To the contrary, Khan clearly teaches that the drop-in heat spreader 202 is attached to the top side of the die 102 using an epoxy

204 (see FIG. 2A and col. 7, lines 29-31). In addition, Khan fails to teach or suggest anything about a top side thermal dissipation metallization. For at least these reasons the Examiner's rejection of claim 14 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Khan should be withdrawn.

V. Claim 18

Claim 18 is rejected under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo. In his rejection of claim 18, the Examiner has stated that Kunikiyo "shows the step of metallurgically bonding a top heat spreader of the package (e.g., 31) to the top side thermal dissipation metallization of the singulated die (dummy pattern 25a)." Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31, as recited in claim 18. For at least these reasons the Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo should be withdrawn.

VI. Claims 19 and 20

Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang. Each of claims 19 and 20 incorporates the features of claim 18. Wang does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 18. To the contrary, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53). For at least these reasons the Examiner's rejection of claims 19 and 20 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang should be withdrawn.

Respectfully submitted,

Date: March 14, 2006



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